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10/758,033	01/16/2004	Kunio Kanda	392.1861	6141

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EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,033	KANDA ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/5/2006 have been fully considered but they are not persuasive. The IRQ processors 45 located within processing systems 1 and 3 of Sone do in fact incorporate all of the limitations argued in claims 1, 3, 5, and 6 and further the limitations in newly added claims 7-9, as discussed below.

In response to Applicant's argument concerning Claim 1, Sone discloses a device for transmitting a wired OR signal between two systems (abstract), each system comprising:

Output means for switching (the examiner interprets the term "switching" to mean the act of changing states [e.g. from low to high or from high to low], which is clearly taught in Sone) between a first state (ie. the low level) in which the system outputs a signal state of the wired OR signal line (the wired OR signals are active-low) and a second state (ie. the high level) in which the system outputs a negate state of the wired OR signal line (Column 10, lines 38-42 [low] and lines 46-50 [high]), and outputting either state to the other system (abstract, Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A; ie. the sending of the IRQ packet from the primary system to the secondary system indirectly causes the secondary –IRQn line to be switched to the corresponding state [see steps 2 and 4 of Figure 21A]);

Switching control means for switching an output state of said output means (Column 10, lines 38-42 and 46-50; ie. the peripheral adapter in the primary system has

the ability to switch between a low state and high state and correspondingly send that state to the secondary system); and

An assert mechanism that maintains the wired OR signal line in an asserted state (ie. the active [low] state) in response to an asserted state transferred by the output means of the other system (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]).

In response to Applicant's argument concerning Claim 3, Sone discloses a device for transmitting a wired OR signal between two systems (abstract), each system comprising:

Output means for outputting the signal state of a wired OR signal line to the other system (abstract, Column 10, lines 38-42 [low] and lines 46-50 [high]);

Switching and outputting means for switching between the first state (ie. the low state) where the signal state transmitted by the output means in the other system is output and the second state (ie. the high state) where negate state is output, and outputting the switched state (Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A);

Switching and controlling means for switching the output of said switching and outputting means (Column 10, lines 38-42 and 46-50; ie. the peripheral adapter in the

primary system has the ability to switch between a low state and high state and correspondingly send that state to the secondary system); and

An assert mechanism that switches the wired OR signal line between an asserted state (ie. low state) or a negate state (ie. high state) according to the output state of said switching and outputting means (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]).

In response to Applicant's argument concerning Claims 5 and 6, Sone discloses a method for communicating wired OR signal between two systems (abstract), in which each system comprises output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line (abstract, Column 10, lines 38-42 [low] and lines 46-50 [high]), and outputting either state to the other system (abstract, Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A), and assert means for maintaining the wired OR signal line in the system in an asserted state in response to an assert signal from the output means of the other system (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]), the method comprising:

switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state (Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A);

processing a device (ie. this is interpreted by the examiner as servicing the device's [the peripheral adapter's] interrupt request) that has brought the wired OR signal line in said other system into the asserted state, after the switching (Column 10 lines 45-46; ie. executing a corresponding interrupt service routine in Sone is considered equivalent to processing a device in the current application); and

switching each of said output means to the second state (ie. the high state), verifying the negate state of the wired OR signal lines in the two systems (ie. the shadow registers 46 in each of the IRQ processors 45 in the primary and second system act as verification of the signal state in the other system, since the shadow registers show the state of the other system [they are toggled each time the state changes the other system]), and then switching each of said output means to the first state (ie. the low state), after finishing the processing of the device (Figure 20, Column 10, lines 38-54; ie. the –IRQn line starts at the high state in both devices while running a process, then switches to the low state [see time marker A] after finishing the currently running process in order to service the Interrupt handling routine).

Therefore, the rejection to Claims 1-6 as being anticipated by Sone stands, to the extent it has been claimed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Sone et al. ("Sone") (U.S. Patent No. 5,524,217).

Regarding Claim 1, Sone discloses a device for transmitting a wired OR signal between two systems (abstract), each system comprising:

Output means for switching (the examiner interprets the term "switching" to mean the act of changing states [e.g. from low to high or from high to low], which is clearly taught in Sone) between a first state (ie. the low level) in which the system outputs a signal state of the wired OR signal line (the wired OR signals are active-low) and a second state (ie. the high level) in which the system outputs a negate state of the wired OR signal line (Column 10, lines 38-42 [low] and lines 46-50 [high]), and outputting either state to the other system (abstract, Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A);

Switching control means for switching an output state of said output means (Column 10, lines 38-42 and 46-50; ie. the peripheral adapter in the primary system has

the ability to switch between a low state and high state and correspondingly send that state to the secondary system); and

An assert mechanism that maintains the wired OR signal line in an asserted state (ie. the active [low] state) in response to an asserted state transferred by the output means of the other system (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]).

Regarding Claim 2, Sone discloses wherein said switching control means comprises a register controlled by a processor in the system (abstract, Column 3, lines 28-32), and said output means comprises:

A mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value (Figure 23, items 46a and 54, Column 13, lines 7-67); and

A transmission mechanism that transfers an output from said mask mechanism to the other system (Figure 23, item 49, Column 13, lines 31-34).

Regarding Claim 3, Sone discloses a device for transmitting a wired OR signal between two systems (abstract), each system comprising:

Output means for outputting the signal state of a wired OR signal line to the other system (abstract, Column 10, lines 38-42 [low] and lines 46-50 [high]);

Switching and outputting means for switching between the first state (ie. the low state) where the signal state transmitted by the output means in the other system is output and the second state (ie. the high state) where negate state is output, and outputting the switched state (Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A);

Switching and controlling means for switching the output of said switching and outputting means (Column 10, lines 38-42 and 46-50; ie. the peripheral adapter in the primary system has the ability to switch between a low state and high state and correspondingly send that state to the secondary system); and

An assert mechanism that switches the wired OR signal line between an asserted state (ie. low state) or a negate state (ie. high state) according to the output state of said switching and outputting means (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]).

Regarding Claim 4, Sone discloses wherein said switching and controlling means is composed of a register controlled by a processor in the system (abstract, Column 3, lines 28-32), and said switching and outputting means is composed of a mask mechanism which switches to the first state when said register has a predetermined value and switches to the second state when the register has a value

other than the predetermined value (Figure 23, items 46a and 54, Column 13, lines 7-67).

Regarding Claim 5, Sone discloses a method for communicating wired OR signal between two systems (abstract), in which each system comprises output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line (abstract, Column 10, lines 38-42 [low] and lines 46-50 [high]), and outputting either state to the other system (abstract, Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A), and assert means for maintaining the wired OR signal line in the system in an asserted state in response to an assert signal from the output means of the other system (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]), the method comprising:

switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state (Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A);

processing a device (ie. this is interpreted by the examiner as servicing the device's [the peripheral adapter's] interrupt request) that has brought the wired OR signal line in said other system into the asserted state, after the switching (Column 10 lines 45-46; ie. executing a corresponding interrupt service routine in Sone is considered equivalent to processing a device in the current application); and

switching each of said output means to the second state (ie. the high state), verifying the negate state of the wired OR signal lines in the two systems (ie. the shadow registers 46 in each of the IRQ processors 45 in the primary and second system act as verification of the signal state in the other system, since the shadow registers show the state of the other system [they are toggled each time the state changes the other system]), and then switching each of said output means to the first state (ie. the low state), after finishing the processing of the device (Figure 20, Column 10, lines 38-54; ie. the –IRQn line starts at the high state in both devices while running a process, then switches to the low state [see time marker A] after finishing the currently running process in order to service the Interrupt handling routine).

Regarding Claim 6, Sone discloses a method for transmitting wired OR signal between two systems (abstract), in which each system comprises output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line (abstract, Column 10, lines 38-42 [low] and lines 46-50 [high]), and outputting either state to the other system (abstract, Column 10, lines 55-56 and lines

58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A), and assert means for maintaining the wired OR signal line in the system in an asserted state in response to an assert signal from the output means of the other system (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A]), the method comprising:

switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state (Column 10, lines 55-56 and lines 58-62, this is further described by example in Column 11 line 64 – Column 12 line 14 with regard to Figure 21A);

processing a device (ie. this is interpreted by the examiner as servicing the device's [the peripheral adapter's] interrupt request) that has brought the wired OR signal line in said other system into the asserted state, after the switching (Column 10 lines 45-46; ie. executing a corresponding interrupt service routine in Sone is considered equivalent to processing a device in the current application); and

switching each of said output means to the second state (ie. the high state), verifying the negate state of the wired OR signal lines in the two systems (ie. the shadow registers 46 in each of the IRQ processors 45 in the primary and second system act as verification of the signal state in the other system, since the shadow registers show the state of the other system [they are toggled each time the state

changes the other system]), and then switching each of said output means to the first state (ie. the low state), after finishing the processing of the device (Figure 20, Column 10, lines 38-54; ie. the –IRQn line starts at the high state in both devices while running a process, then switches to the low state [see time marker A] after finishing the currently running process in order to service the Interrupt handling routine).

Regarding Claim 7, Sone discloses a method for transmitting a wired logic circuit signal between two systems, comprising:

Driving a first system device to assert a first wired signal line to a low level in a first system (Figure 21A, step 1, Column 11 line 64 – Column 12 line 1); and

Causing the asserted state of the first signal line to be transferred to a second wired signal line of a second system, which transfers the asserted state of the second line to the first line, thereby maintaining the asserted states of the first and the second wired signal lines after the first system device is turned off to stop asserting the first wired signal line (Figure 21A, Column 11 line 64 – Column 12 line 14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A], Sone also teaches that secondary -IRQn line can send it's signal state to the primary system in step 5 if necessary).

Regarding Claim 8, Sone discloses changing a value in a first register in the first system from a predetermined value (Figure 22B, step 2, Column 13, lines 1-3; ie. the

secondary system changes from the low state to the high state [step 1], and thereafter causes shadow register 46 of the primary system to toggle to the high state also); and

Transferring a negate state (ie. high state) from the first system to the second system, based on the change from the predetermined value (Figure 22B, step 3, Column 13, lines 3-6; ie. the primary system sends it's negate state from it's shadow register 46 to the shadow-shadow register 47 of the secondary system);

Wherein the second wired signal line is thereafter not asserted (Figure 22B, see box labeled "ON –IRQn BUS" under "Secondary", Column 12, lines 62-65; ie. the signal on the –IRQn wired-OR bus in the secondary system is in the negated [high] state).

Regarding Claim 9, Sone discloses a device for transmitting a wired logic circuit signal between a first system and a second system, comprising:

A first mask mechanism and a first transmission mechanism outputting and transmitting an asserted state (ie. a low state) of a first wired signal line of the first system from the first system to the second system (Figure 21A, step 2, Column 11 line 64 – Column 12 line 1);

An assert mechanism of the second system asserting a second wired signal line of the second system as a result of the transmission of the asserted state from the first system; a second mask mechanism and a second transmission mechanism outputting and transmitting an asserted state of the second wired signal line to the first system (Figure 21A, step 4 and 5, Column 12, lines 1-14; ie. when the asserted [low] state is output from the primary system [see step 1 of Figure 21A], the wired OR –IRQn line of

the secondary system in turn goes to [and is maintained at] an asserted [low] state [see step 4 of Figure 21A], Sone also teaches that secondary -IRQn line can send it's signal state to the primary system in step 5 if necessary); and

An assert mechanism of the first system driven to maintain the first wired signal line in the asserted state (Figure 21A, see box labeled "ON –IRQn BUS" under "Primary", Column 11 line 64 – Column 12 line 14; ie. the signal on the –IRQn wired-OR bus in the primary system is in the asserted [low] state); and

A register of the first system (Figure 5B, item 46);

Wherein if a value in the register changes from a predetermined value, a negate state is output and transferred from the first system to the second system so the first wired signal line and the second wired signal line are brought into a negate state (Figure 22B, step 3, Column 13, lines 3-6; ie. in this embodiment, the primary system sends it's negate state from it's shadow register 46 to the shadow-shadow register 47 of the secondary system, causing both the primary and secondary system to be in the negate [high] state).

Prior Art of Record

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nishioka (U.S. Patent No. 4,799,148) discloses an interrupt control system having a processor for determining service priority among a plurality of modules according to an interrupt status table. D'Amico et al. (U.S. Patent No. 4,796,176) discloses a method of interrupt handling in a dual processor system.

Sarangdhar et al. (U.S. Patent No. 5,659,689) discloses a method and apparatus for transmitting information on a wired-or bus. Kumar et al. (U.S. Patent Publication No. 2002/0087765) discloses a method and system for completing purge requests or the like in a multi-node multiprocessor system. Delvaux (U.S. Patent No. 6,608,571) discloses a system and method for communicating over a one-wire bus. Friel et al. (U.S. Patent No. 6,697,897) discloses a data communication interface between host and slave processors. Sakaue (U.S. Patent No. 6,754,205) discloses a switching element and packet switch. Jurasek et al. (U.S. Patent No. 6,954,451) discloses a distributed time-multiplexed bus architecture and emulation apparatus.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

fmz

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
5/8/06